

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 1. (Previously presented): A method for manufacturing a semiconductor
2 power device, comprising:
3 identifying an active region on a semiconductor die, the active region having a
4 central portion, a first peripheral portion disposed about a periphery of said central portion, and a
5 second peripheral portion disposed about a peripheral region of said first peripheral portion;
6 identifying a first region in said central portion of said active region;
7 identifying a second region in said first peripheral portion of said active region;
8 identifying a third region in said second peripheral portion;
9 fabricating active cells in accordance with a first cell design in said first region;
10 fabricating active cells in accordance with a second cell design in said second
11 region, wherein an operational current density of said active cells fabricated according to said
12 second cell design is greater than that of said active cells fabricated according to said first cell
13 design, and
14 fabricating active cells in accordance with a third cell design in said third region,
15 wherein the operational current density of said active cells fabricated according to said third cell
16 design is greater than that of said active cells fabricated according to said second cell design.

1 2. (Original): The method of claim 1 wherein said first cell design and said
2 second cell design include cell dimensions such that a cell density of said first region is different
3 from that of said second region.

1 3. (Original): The method of claim 1 wherein said first cell design includes
2 at least one physical dimension different from that included in said second cell design.

1 4. (Original): The method of claim 3 wherein said physical dimension
2 includes a channel width.

1 5. (Original): The method of claim 4 wherein said physical dimension
2 includes a cell die area.

1 6. (Original): The method of claim 1 wherein said first cell design includes a
2 material composition for cells that is different from that of said second cell design.

1 7. (Previously presented): The method of claim 1 wherein said first cell
2 design differs from said second cell design with respect to cell density.

1 8. (Original): The method of claim 1 wherein said first cell design differs
2 from said second cell design with respect to source resistance.

1 9. (Original): The method of claim 1 wherein said first cell design differs
2 from said second cell design with respect to transconductance.

1 10. (Original): The method of claim 1 wherein said first cell design differs
2 from said second cell design with respect to gain.

1 11. (Original): The method of claim 1 wherein said first cell design differs
2 from said second cell design with respect to threshold voltage.

1 12. (Original): The method of claim 1 wherein said first cell design and said
2 second cell design are field effect transistors.

1 13. (Original): The method of claim 1 wherein said first cell design and said
2 second cell design are memory cells.

1 14. (Previously presented): A semiconductor power device fabricated in
2 accordance with the method of claim 1.

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PATENT

15-17. (Canceled)